19. The method of claim 15, wherein the silicon carbide passivation layer is deposited by the method for depositing the silicon carbide barrier layer.

20. The method of claim 15, wherein the silicon carbide barrier layer is deposited using an RF power supply supplying a power density of about 8.6 to about 14.3 watts per square inch to an anode and cathode in the chamber.

21. The method of claim 15, wherein the silicon carbide barrier layer is deposited with a methylsilane flow rate of between about 100 to about 500 sccm, a helium or argon gas flow rate of between about 1000 to about 2000 sccm, a chamber pressure of about 6 to about 8 Torr, an RF power source supplying a power density of about 8.6 to about 14.3 watts per square inch to an anode and cathode in the chamber, a substrate surface temperature of between about 200°C to about 400°C, and a showerhead to substrate surface spacing of between about 300 to about 600 mils.

22. (Amended) The method of claim 15, wherein the alkylsilane is selected from the group of methylsilane, dimethylsilane, trimethylsilane, and combinations thereof.

REMARKS

This is intended as a full and complete response to the Office Action dated January 28, 2003, having a shortened statutory period for response set to expire on April 28, 2003. Claims 15-22 are pending in this application. Claims 15-22 were considered and stand rejected. Claims 15-22 have been amended to correct matters of form. Applicants believe that no new matter has been introduced in this response.

Claims 15-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of *Endo, et al.* (U.S. Patent No. 4,532,150), Europe '440 (*Loboda, et al.*, EP 725,440), and Applicants' admitted prior art and further in view of either *Naik, et al.* (U.S. Patent No. 6,245,662) and *Yau, et al.* (U.S. Patent No. 6,054,379) or *Chiang, et al.* 5,817,572).

The Examiner asserts that it would have been within the scope of one or ordinary skill in the art to combine the teachings of *Endo et al.* '150, Applicants' admitted prior art, and Europe '440 with either *Naik et al.*, *Yau, et al.*, or *Chiang* to enable the formation of the structure of Figure 1. Applicants respectfully traverse this rejection.

Naik et al., *Yau, et al.*, and the present application were commonly owned by Applied Materials, Inc., at the time the invention of the present application was made as indicated by an enclosed statement of common ownership, and *Naik et al.* and *Yau, et al.* are available as a reference only under the provisions of §102(e). Therefore, *Naik et al.* and *Yau, et al.* are not prior art under the new §103(a) rule, which is applied to this Examiner's Office Action submitted after the Continued Prosecution Application (CPA) filed on December 5, 2002, for Patent Application Serial No. 09/165,248. Withdrawal of the rejections based on *Naik et al.* and *Yau, et al.* is respectfully requested.

Endo et al. '150 discloses a process for depositing silicon carbide on a substrate. The substrate may be metallic, such as aluminum material. Europe '440 discloses depositing a silicon carbon barrier layer on a metal surface, between two metal layers to prevent interlayer diffusion, or between a metal and a dielectric material to prevent diffusion of the metal into the dielectric material and insulate layers of wiring.

Chiang discloses a first patterned dielectric layer formed over the semiconductor substrate and has a first opening filled with a metal, and then another patterned dielectric layer is formed over the first dielectric layer and has a second opening over at least a portion of the conductive metal. A dielectric etch stop may be formed over the over the first patterned dielectric layer and conductive material prior to forming the other patterned dielectric layer. The dielectric etch stop is disposed between formed and metallized damascene structures. Thus, *Chiang* teaches away from depositing a silicon carbide barrier layer on the substrate, depositing a first dielectric layer on the silicon carbide layer, depositing a silicon carbide etch stop, patterning the silicon carbide etch stop, depositing a second dielectric layer on the silicon carbide etch stop, etching the first dielectric layer and the second dielectric layer to form a feature definition.

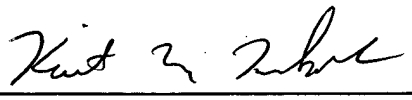
Thus the combination of *Endo et al.* '150, Applicants admitted prior art as indicated by the Examiner in the paper mailed March 20, 2002, and Europe '440 with *Chiang* does not teach, show, or suggest depositing a silicon carbide barrier layer on

the substrate by a method comprising introducing an alkylsilane and a noble gas into a chamber, initiating a plasma in the chamber, and reacting the alkylsilane in the presence of the plasma to form silicon carbide, depositing a first dielectric layer on the silicon carbide barrier layer, depositing a silicon carbide etch stop having an etch selectivity ratio of at least about 40 to 1 on the first dielectric layer by a method comprising introducing an alkylsilane and a noble gas into a chamber, initiating a plasma in the chamber, and reacting the alkylsilane in the presence of the plasma to form silicon carbide, patterning the silicon carbide etch stop, depositing a second dielectric layer on the silicon carbide etch stop, etching the first dielectric layer and the second dielectric layer to form a feature definition, as recited in claim 15, and claims dependent thereon. Withdrawal of the rejection is respectfully requested.

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action. Accordingly, allowance of the claims is respectfully requested.

In conclusion, the references cited by the Examiner, neither alone nor in combination, teach, show, or suggest the method or apparatus of the present invention. Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

15. (Fourth Amendment) A method for processing a substrate, comprising:

depositing a silicon carbide barrier layer on the substrate by a method comprising:

introducing an alkylsilane and a noble gas into a chamber;

initiating a plasma in the chamber; and

reacting the alkylsilane in the presence of the plasma to form silicon carbide;

depositing a first dielectric layer on the silicon carbide barrier layer;

depositing a silicon carbide etch stop having an etch selectivity ratio of at least about 40 to 1 on the first dielectric layer by a method comprising:

introducing an alkylsilane and a noble gas into a chamber;

initiating a plasma in the chamber; and

reacting the alkylsilane in the presence of the plasma to form silicon carbide;

patterning the silicon carbide etch stop;

depositing a second dielectric layer on the silicon carbide etch stop;

etching the first dielectric layer and the second dielectric layer to form a feature definition;

depositing a tantalum nitride barrier layer in the feature definition;

depositing a copper layer over the tantalum nitride barrier layer to fill the feature definition; and

depositing a silicon carbide passivation layer on the copper layer.

22. (Amended) The method of claim 15, wherein the alkylsilane is [derived from a common methylsilane] selected from the group of methylsilane, dimethylsilane, trimethylsilane, and combinations thereof.